**ASSIGNMENT- 2**

**CIS-580 INTRO TO COMPUTER ARCHEITECTURE SECTION 50**

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**CHAPTER: 3**

**1 ANS)**

Given Boolean expression X = (X AND Y) OR (X AND NOT Y)

**AND** operator is executed **TRUE** when both inputs are **TRUE** or else **FALSE.**

**OR** operator is executed **TRUE** either one Input is **TRUE** or else **FALSE.**

**NOT** operator is executed then its result in **TRUE** is any of the inputs is **FALSE** else results is **FALSE**.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **X** | **Y** | **NOT Y** | **X AND Y** | **X AND NOT Y** | **(X AND Y) OR (X AND NOT Y)** |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |

**2 ANS)**

**AND** operator is executed **TRUE** when both inputs are **TRUE** or else **FALSE.**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **X** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

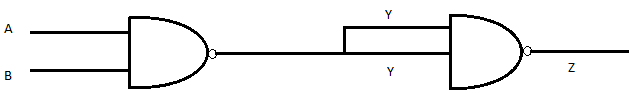
**NAND GATE** operator executed **TRUE** if any one of the input is **False** or else it is **FALSE**.

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| **0** | 0 | 1 |
| **0** | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NAND** output can be used to construct **AND** output.

|  |  |  |
| --- | --- | --- |
| **Y** | **Y** | **Z** |
| 1 | 1 | 0 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

TWO **NAND GATES** can be used to perform the **AND FUNCTION.**



**3 ANS)**

Circuit

The Logical diagram which is presented can be used to derive the logical statement for C and D as follows:

C=NOT (NOT (A AND (NOT (A AND B))) AND (NOT ((NOT (A AND B)) AND B)))

This can be simplified by using a truth table.

|  |  |  |
| --- | --- | --- |
| A | B | X=NOT (A AND B) |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

X is then fed to two NAND gates each having A and B other inputs. And C is the output of the NAND operation on the output of these two NAND gates. The truth table is given below

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | X | Y=NOT (A AND X ) | Z=NOT(B AND X) | C=NOT (Y AND Z) |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |

Now, the logical expression for C can be derived as follows:

C= ( AND B) OR (A AND )

= A X OR B

The logical expression for D can be derived from the diagram as follows:

D=NOT ( NOT(A AND B))

= A AND B

Therefore, these expressions of C and D show that the diagram represents a half adder.

**4 ANS)**

**As** 4x3 memory ,256x8 memory would use two and gates for chip select (CS) and output enable (OE).

The 4x3 memory uses 2AND gates per select line for a word. For 256x8 memory would use 512 AND gates as there are 256 words.

The 4x3 memory would uses 1 AND gates for each data bit. Thus, 256x8 memory would use 2048 AND gates as there 256x8=2048bits.

As 4x3 memory, 256x8 memory also use one or gates for one or gates for one bit in the word. Thus, 256x8 memory would use 8 or gates as there are 8 bits per word.

Hence the total number of and gates required is 2+512+2048=2562 and the number of or gates required is 8.

**5 ANS)**

Each and every chip has 1 bit of data. The number of chips required for the 32-bit data is 32. This show that the chips can be used as parallel.

Thus, the least memory provided by 32 chips will be 32 megabits.

One byte consists of 8bits. The 32 megabits can be converted in and as

32 megabits **/**8 = 4megabytes.

Hence, the 32-bit data bus would provide at least 4Megabytes of memory.

**6 ANS)**

|  |  |
| --- | --- |
| **MEMORY BUS** | **PCI BUS** |
| It is also called as system bus. | It doesn’t have another name. |
| It is mainly connecting the CPU to the memory and level 2 cache. | PCI bus connect to system bus through bridge. |
| It mainly interconnects the processor with the memory system and input/output bus | It is a single bus mainly connects the major component of system. |
| It works more faster than PCI bus. | It is a slower bus. Its working like hard disk and sound cards. |
| It is mainly made up of two parts, that is data bus and address bus. | Its combining the functions of data bus. |

**7 ANS)**

* Single layers of cache will take time to do process.
* When the processors cache is large than the latency rate will be high.
* Using multiple level of cache will increase the performance of the system.
* Possible to store more data.
* Multiple levels of cache can avoid aliasing problems.
* It improves the average memory access time of a system.